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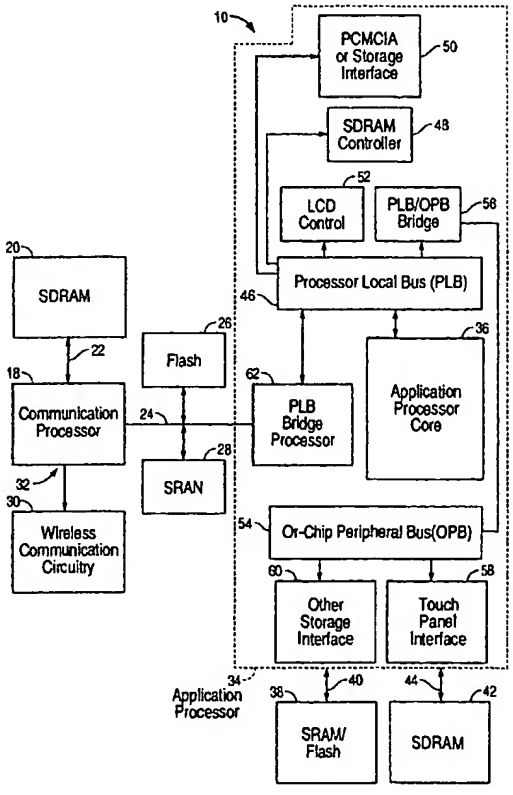
(54) Title: LOW POWER DUAL PROCESSOR ARCHITECTURE FOR MULTI MODE DEVICES



(57) Abstract: A mobile computing device with multiple modes, for example, wireless communication and personal computing, has an application processor and a communication processor. In the computing mode, the application processor is the master processor. In the communication mode, the application processor is deenergized to conserve battery power, with the communication processor functioning as the master processor by accessing the device's peripheral bus using the memory interface of the communication processor.

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LOW POWER DUAL PROCESSOR ARCHITECTURE FOR MULTI MODE DEVICES

I. Field of the Invention

[0001] The present invention relates generally to multi mode devices such as wireless telephones that can also undertake ancillary computer functions.

II. Background of the Invention

[0002] Multi mode mobile computing devices have been proposed which have multiple capabilities. For example, mobile telephones might be expected to undertake personal computing tasks now undertaken by notebook computers, in addition to their communication functions.

[0003] As recognized herein, multiple processors might be required to support multiple modes of operation. As also recognized herein, using the same internal operation independent of the operational mode means that a main processor typically functions as a master device that controls peripheral devices and that treats the other device processors (e.g., a telephone modem processor) as peripherals. Such a design requires that the main processor be active in all modes, including, e.g., the main processor needs to be active in the telephone mode, in which the modem processor is active, simply to provide the modem processor access to device hardware (e.g., a data display, non volatile storage, audio input/output) that is controlled by the main processor. In other words the main processor is here simply mediating on behalf of the modem processor, because the hardware architecture does not allow the modem processor direct access to some of the hardware resources in the device.

[0004] As understood herein, it would be advantageous to minimize when possible, the use of hardware intermediaries (such as the main processor in the example above) to allow power efficient execution of tasks, to conserve the battery. Moreover by use of methods described in this invention it may be possible to power off processors that don't need to serve such intermediary role further extending device battery life. Furthermore, requiring a single main processor to always function as a device master means that software and software changes that might apply only to a modem processor must be coordinated or otherwise integrated with the main processor as well, complicating software management.

In particular the large base of software presently available for cellular phone type devices, which functions on the modem processor cannot be used unchanged in a device in which the modem processor is a peripheral to a main application processor. The present invention can allow the reuse of this large base legacy of application software by architecting the hardware so that it appears to the legacy software as it would in current single processor devices.

SUMMARY OF THE INVENTION

[0005] A multi mode mobile device includes a housing holding a battery and a communication processor that may be embodied in a module configured to facilitate wireless communication using the device. The communication processor module is supported on the housing and is powered by the battery. An application processor that may be embodied in a module is configured to execute applications is also supported on the housing and powered by the battery. A module in this description means a collection of hardware, assembled of discrete components or within an integrated circuit package, that performs a function through coordinated use of its hardware components. In particular a communication processor module consists of a communications processor core in addition to other hardware resources that function as peripherals of the communications processor (for example Qualcomm's MSM 3300, 5100, 5500 which an ARM processor core are in the current view communications processor modules). Similarly in the current view an application processor module consists of an application processor core together with assisting hardware (for example Qualcomm's MSP1000 or IBM's 405GP which have ARM and PowerPC processor cores are examples of application processor modules). In accordance with this aspect, the device has a communication mode and a computing mode, and when the device is in the communication mode, a core of the application processor is not energized. The application processor core is energized, however, when the device is in the computing mode.

[0006] Preferably, the communication processor module is associated with a memory bus that communicates with one or more memory devices and the application processor module is associated with a processor local bus (PLB). The preferred memory bus communicates with the PLB through hardware interfaces between the communication processor module

and the application processor module. More specifically, the preferred memory bus communicates with a PLB bridge processor to facilitate the communication processor functioning as a master of the PLB. The communication processor can thereby access peripheral hardware associated with the PLB.

[0007] In another aspect, a multi mode mobile device includes a housing holding a battery and a communication processor configured to facilitate wireless communication using the device. The communication processor is supported on the housing and is powered by the battery. An application processor is configured to execute applications, and the application processor is supported on the housing and powered by the battery. The device has at least a communication mode and a computing mode, and when the device is in the communication mode, the communication processor functions as a master processor.

[0008] In still another aspect, a method for effecting mobile computing includes supporting an application processor and a communication processor in a housing. The method also includes selectively establishing one of the processors as a master processor based on a mode of operation.

[0009] The details of the present invention, both as to its structure and operation, can best be understood in reference to the accompanying drawings, in which like reference numerals refer to like parts, and in which:

While the description of the invention is presented in the context of distinct communication and application processor modules, it is recognized that this is only done for clarity of exposition. In particular it is envisaged that the communication and application processor modules could be realized on the same integrated circuit module, whether this be through a multi-chip-module packaging technique or through the design of the entire circuit as a single chip with the both (application and communications) processor cores on it.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0010] Figure 1 is schematic diagram of a preferred non-limiting multi mode mobile computing device;

[0011] Figure 2 is a block diagram of a preferred non-limiting implementation of the present multi mode mobile device architecture; and

[0012] Figure 3 is a flow chart illustrating the logic of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0013] Referring initially to Figure 1, a mobile multi mode computing device is shown, generally designated 10. In an exemplary non-limiting embodiment, the device 10 can be used to undertake wireless voice and/or data communication as well as personal computing application-based functions, such as but not limited to word processing. In any case, the device 10 includes a preferably lightweight portable housing 12 that holds the components discussed herein. A battery 14 can be engaged with the housing 12 to provide a source of power to the components disclosed below. The battery 14 preferably is rechargeable in accordance with portable computing principles known in the art, but when the device 10 is not connected to an electrical outlet, the battery 14 is the sole source of power to the components of the device 10.

[0014] A mode selector 16 can be provided on the housing 12. The mode selector 16 can be a user-manipulable input device to select the operational mode of the device 10, e.g., communication or computing. The mode selector 16 can be implemented in any number of ways, e.g., it can be a switch, or a portion of a touchscreen display that is used in conjunction with appropriate software to select the mode, or other equivalent input structure. Or, the mode selector 16 can be automatically implemented by software responsive to the user's activities, e.g., if the user starts to dial a number the mode selector can be software that automatically configures the device 10 in the communication mode.

[0015] Now referring to Figure 2, the device 10 includes a communication processor 18, preferably a type of processor referred to as a mobile system modem (MSM) that can access synchronous dynamic random access memory (SDRAM) 20 over, e.g., a 16/32 bit bus 22 and that can be implemented in a communication processor module. Also, the

communication processor 18 can access, using, for instance, a 16 bit memory interface bus 24, MSM flash memory 26 and MSM static random access memory (SRAM) 28. Communication-related applications, such as the present assignee's "BREW" applications, can be stored in one or more of the memories 20, 26, 28 for execution thereof by the communication processor 18.

[0016] As also shown in Figure 2, the communication processor 18 accesses wireless communication circuitry 30 to effect wireless communication in accordance with means known in the art. In other words, the communication processor 18, associated memories 20, 26, and 28, and circuitry 30 establish a wireless voice and/or data communication portion, generally designated 32.

[0017] In one non-limiting embodiment, the communication portion 32, also referred to as a "mobile station ("MS"), is a mobile telephone-type device made by Kyocera, Samsung, or other manufacturer that uses Code Division Multiple Access (CDMA) principles and CDMA over-the-air (OTA) communication air interface protocols such as defined in but not limited to IS-95A, IS-95B, WCDMA, IS-2000, and others to communicate with wireless infrastructure, although the present invention applies to any wireless communication device.

[0018] For instance, the wireless communication systems to which the present invention can apply, in amplification to those noted above, include GSM, Personal Communications Service (PCS) and cellular systems, such as Analog Advanced Mobile Phone System (AMPS) and the following digital systems: CDMA, Time Division Multiple Access (TDMA), and hybrid systems that use both TDMA and CDMA technologies. A CDMA cellular system is described in the Telecommunications Industry Association/Electronic Industries Association (TIA/EIA) Standard IS-95. Combined AMPS and CDMA systems are described in TIA/EIA Standard IS-98. Other communications systems are described in the International Mobile Telecommunications System 2000/Universal Mobile Telecommunications Systems (IMT-2000/UM), standards covering what are referred to as wideband CDMA (WCDMA), cdma2000 (such as cdma2000 1x or 3x standards, for example) or TD-SCDMA.

[0019] Still referring to Figure 2, a main processor 34 that can be embodied in a module holds an application processor core 36, which in one non-limiting illustrative embodiment

can be an IBM 405 LP processor or equivalent. While Figure 2 shows that the processors 18, 36 can be on separate chips from each other, it is to be appreciated that they can also be disposed on the same chip.

[0020] The application processor core 36 accesses one or more software applications that can be stored in various memories to execute the applications. For example, the application processor core 36 can access an SRAM/Flash memory 38 over, e.g., a 16-bit memory bus 40, and it can also access an SDRAM memory 42 (where software applications typically will be preferentially stored) over a preferably 32-bit bus 44.

[0021] Figure 2 also shows that the application processor core 36 accesses a processor local bus (PLB) 46. In one non-limiting embodiment, the PLB bus 46 can be a 64-bit bus. Various supporting devices and peripherals are accessed by the application processor core 36 using the PLB 46 in accordance with principles known in the art. For example, the PLB 46 (and, hence, application processor core 36) can be connected to a SDRAM controller 48 for controlling the SDRAM memory 42. Also, the PLB 46 can communicate with a personal computer memory card interface architecture (PCMCIA) interface or other storage interface 50. Moreover, the PLB 46 (and, hence, application processor core 36) can be connected to a liquid crystal display (LCD) controller 52, which drives an LCD display that can be provided on the housing of the device 10.

[0022] In addition to the components discussed above, the application processor 34 which bears the application processor core 36 can also hold an on-chip peripheral bus (OPB) 54 which in one non-limiting embodiment can be a 32 bit bus. The OPB 54 is connected to the PLB 46 through a PLB/OPB bridge device 56. The bridge device 56 can translate 32 bit data to 64 bit data and vice versa. Various peripheral devices can communicate with the OPB 54. By way of non-limiting examples, a touch panel interface 58 can be connected to the OPB 54. Also, other storage interfaces 60 can be connected to the OPB 54. Further non-limiting examples of peripheral devices that can be connected to the OPB 54 include a USB, a UART, an interrupt (UC), and an AC97 device.

[0023] In accordance with the present invention, the communication processor 18 can also communicate with the PLB 46 over its memory interface 24. Specifically, as shown in Figure 2, in one exemplary embodiment the memory interface 24 of the communication processor 18 is connected to the PLB 46 by a PLB bridge processor 62. In one

implementation, the PLB bridge processor 62 is implemented in hardware by a logic device, such as, e.g., a processor. In this way, the communication processor 18 can access the devices connected to the PLB 46. If desired, the functions of the PLB bridge processor 62 can be implemented by, e.g., a dedicated portion of the communication processor 18.

[0024] Figure 3 shows the logic that is executed by the PLB bridge processor 62 to negotiate which processor 18, 36 controls the peripherals shown in Figure 2. At decision diamond 64 it is determined whether the device 10 is in the communication mode as indicated by, e.g., the mode selector 16 or other user activity discussed above. If not, meaning that the device 10 is in the computing mode, the logic flows to block 66, wherein the PLB bridge processor 62 designates the application processor core 36 to be the master processor in control of the PLB 46 and OPB 54. In this mode, the communication processor 18 can be treated by the application processor core 36 as a peripheral device.

[0025] On the other hand, if the device 10 is in the communication mode, the logic moves from decision diamond 64 to block 68, wherein at least the application processor core 36 of the application processor 34 is deenergized. That is, in the communication mode, according to present principles the application processor core 36 is deenergized. Consequently, the communication processor 18 is assigned (by, e.g., the PLB bridge processor 62) the role of master processor at block 70, controlling the peripheral devices connected to the PLB 46 and OPB 54.

[0026] While the particular LOW POWER DUAL PROCESSOR ARCHITECTURE FOR MULTI MODE DEVICES as herein shown and described in detail is fully capable of attaining the above-described objects of the invention, it is to be understood that it is the presently preferred embodiment of the present invention and is thus representative of the subject matter which is broadly contemplated by the present invention, that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more". All structural and functional equivalents to the elements of the above-described preferred embodiment that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to

be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. '112, sixth paragraph, unless the element is expressly recited using the phrase "means for" or, in the case of a method claim, the element is recited as a "step" instead of an "act".

CLAIMS

WHAT IS CLAIMED IS:

1. A multi mode mobile device, comprising:

a housing holding a battery;

at least one communication processor configured to facilitate wireless communication using the device, the communication processor being supported on the housing and being powered at least in part by the battery; and

at least one application processor configured to execute at least one application, the application processor being supported on the housing and being powered at least in part by the battery,

wherein the device has at least a communication mode and a computing mode, and when the device is in the communication mode, a core of the application processor is not energized.

2. The device of Claim 1, wherein the communication processor is associated with a memory bus communicating with one or more memory devices and the application processor is associated with a processor local bus (PLB), and the memory bus communicates with the PLB.

3. The device of Claim 2, wherein the memory bus communicates with a PLB bridge processor to facilitate the communication processor functioning as a master of the PLB.

4. The device of Claim 3, wherein the communication processor accesses peripheral hardware associated with the PLB.

5. The device of Claim 1, further comprising a PLB bridge processor interposed between the memory bus and PLB.

6. The device of Claim 1, wherein the application processor is energized when the device is in the computing mode.

7. The device of Claim 2, further comprising at least one peripheral hardware component connected to the PLB.

8. The device of Claim 7, wherein the peripheral hardware component is at least one of: a touch panel controller, and a storage interface.

9. A multi mode mobile device, comprising:

a housing holding a battery;

at least one communication processor configured to facilitate wireless communication using the device, the communication processor being supported on the housing and being powered at least in part by the battery; and

at least one application processor configured to execute at least one application, the application processor being supported on the housing and being powered at least in part by the battery,

wherein the device has at least a communication mode and a computing mode, and when the device is in the communication mode, the communication processor functions as a master processor.

10. The device of Claim 9, wherein when the communication processor functions as a master processor, it at least controls at least one peripheral hardware component on the device.

11. The device of Claim 9, wherein when the device is in the communication mode, the application processor is not energized.

12. The device of Claim 9, wherein the communication processor is associated with a memory bus communicating with one or more memory devices and the application

processor is associated with a processor local bus (PLB), and the memory bus communicates with the PLB.

13. The device of Claim 12, wherein the memory bus communicates with the PLB using a PLB bridge processor to facilitate the communication processor functioning as a master of the PLB.

14. The device of Claim 13, wherein the communication processor accesses peripheral hardware associated with the PLB.

15. The device of Claim 14, further comprising a PLB bridge processor interposed between the memory bus and PLB.

16. The device of Claim 11, wherein the application processor is energized when the device is in the computing mode.

17. The device of Claim 10, wherein the peripheral hardware component communicates with the PLB.

18. A method for effecting mobile computing, comprising:

supporting an application processor and a communication processor in a housing; and

selectively establishing one of the processors as a master processor based on a mode of operation.

19. The method of Claim 18, wherein a processor is a master processor at least in part based on its control of at least one peripheral hardware component supported on the housing.

20. The method of Claim 19, comprising undertaking wireless communication using the communication processor in a communication mode with the application processor being deenergized and the communication processor being a master processor.

21. The method of Claim 19, comprising executing at least one application using the application processor in an application mode, wherein the application processor is a master processor and the communication processor is a peripheral processor.

22. The method of Claim 18, further comprising energizing at least one processor using at least one battery.

23. The method of Claim 18, comprising establishing communication between the communication processor and a bus of the application processor using a memory interface of the communication processor.

24. The method of Claim 18, further comprising disposing a PLB bridge processor on the housing to undertake the act of selectively establishing.

25. A system for effecting mobile computing, comprising:

a housing;

application processing means for executing logic, the application processing means being mounted on the housing;

communication processing means for executing logic, the communication processing means being mounted on the housing; and

means for selectively establishing one of the processoring means as a master processor based on a mode of operation.

26. The system of Claim 25, wherein a processing means is a master processor at least in part based on its control of at least one peripheral hardware component supported on the housing.

27. The system of Claim 26, comprising means for undertaking wireless communication using the communication processing means in a communication mode with the application processing means being deenergized and the communication processing means being a master processor.

28. The system of Claim 26, comprising means for executing at least one application using the application processing means in an application mode, wherein the application processing means is a master processor and the communication processing means is a peripheral processor.

29. The system of Claim 25, further comprising means for energizing at least one processor using at least one battery.

30. The system of Claim 25, comprising means for establishing communication between the communication processing means and a bus of the application processing means using a memory interface of the communication processing means.

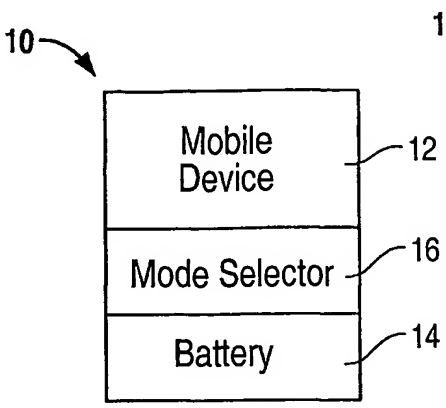
10
Mobile Device
12
Mode Selector
16
Battery
14

FIG. 1

10
PCMCIA or Storage Interface
50
SDRAM Controller
48
52
LCD Control
PLB/OPB Bridge
56
Processor Local Bus (PLB)
46
20
SDRAM
22
26
Flash
36
18
62
Communication Processor
24
PLB Bridge Processor
Application Processor Core
28
SRAN
32
30
Wireless Communication Circuitry
54
Or-Chip Peripheral Bus(OPB)
60
58
Other Storage Interface
Touch Panel Interface
34
Application Processor
40
44
38
42
SRAM/ Flash
SDRAM

FIG. 2

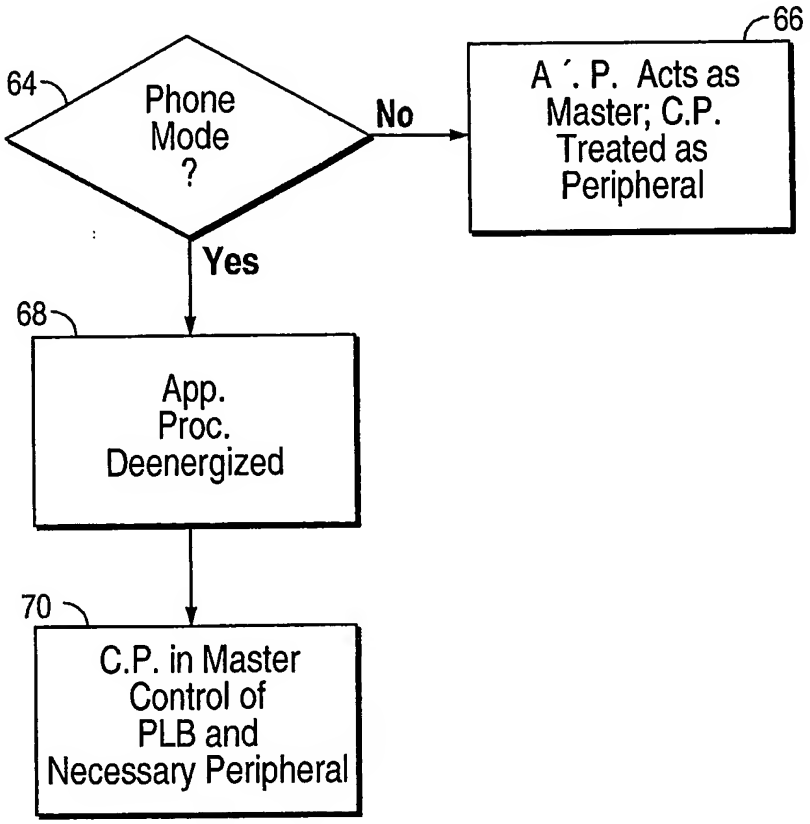
64
Phone Mode ?
No
66
A´. P. Acts as Master; C.P. Treated as Peripheral
Yes
68
App. Proc. Deenergized
70
C.P. in Master Control of PLB and Necessary Peripheral

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/27182

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04M 1/00, H04B 1/38
US CL : 455/556, 550
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 455/556, 550, 556.1, 556.2, 574, 557, 90.1, 90.2, 90.3, 347, 351, 343.1; 701/226; 216/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPAT; US-PGPUB; DERWENT; 455/557.ccls, processor or microprocessor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P --- Y,P	US 2002/0173344 A1 (CUPPS et al) 21 November 2002, fig. 3; fig. 3 item 302, para. 29; fig. 3, item 320, para. 32.	1, 8-11, 16, 18-23, 25-30 --- 2-5, 7, 12-15, 17, 24
Y,E	US 2003/0163798 A1 (HWANG et al) 28 August 2003, para. 4, 31, 32.	2-5, 7, 12-15, 17, 24
A	US 5,487,181 A (DAILEY et al) 23 January 1996, entire document.	1-30
A	US 5,925,092 A (SWAN et al) 20 July 1999, entire document.	1-30

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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